

**A Novel Dimension Reduction Technique For 3D
Capacitance Extraction Of VLSI Interconnects
(Technical Report / Computer Research Laboratory,
UCSC) By Wei Hong**



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Dimensionality reduction - wikipedia, the free

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Dimensionality Reduction Techniques for Face Recognition | InTechOpen, Published on: 2011-07-27. Authors: Shylaja S. Sharath, Balasubramanya Murthy K N and Natarajan S

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